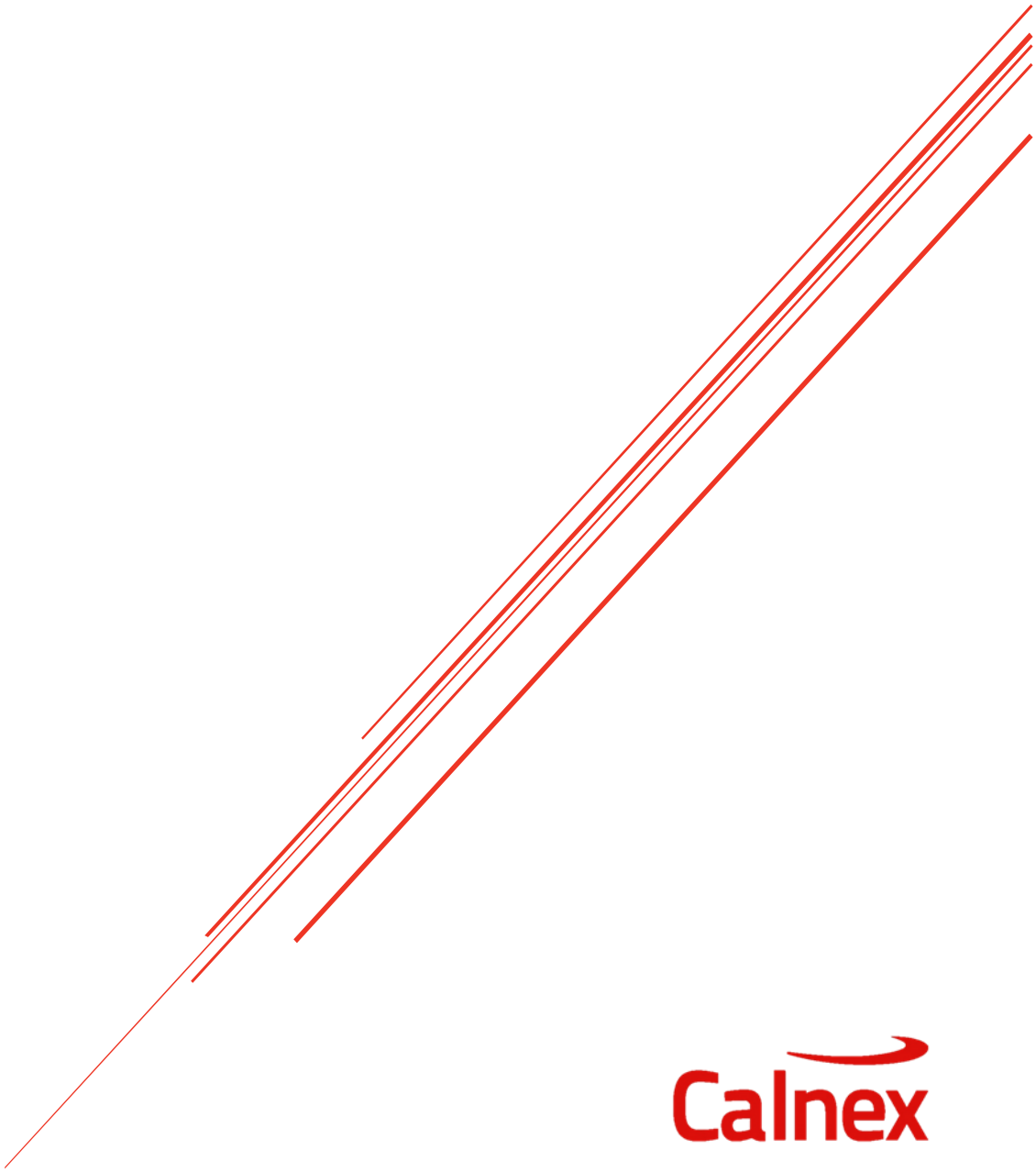
INTERPRETATION OF TIME ERROR RESULTS

Understanding down to the nanosecond level



Calnex

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1pps Measurements

The analysis of 1pps results is specified in ITU-T G.810:

***4.5.13 time error function**: The time error of a clock, with respect to a frequency standard, is the difference between the time of that clock and the frequency standard one. Mathematically, the Time Error function x(t) between a clock generating time T(t) and a reference clock generating time $T_{ref}(t)$ is defined as:*

$$x(t) = \mathrm{T}(t) - \mathrm{T}_{\mathrm{ref}}(t)$$

Consider the case when the output 1pps from the Device Under Test (DUT) is being compared to the 1pps output from the Time Reference. In the example picture below (Fig.1), the DUT lags the Time Reference by time Xnsec. When the 1pps pulse emerges from the DUT, the reference time has moved on by Xnsec. Therefore when the equation above is applied, a negative value is produced, as illustrated in Fig.1.

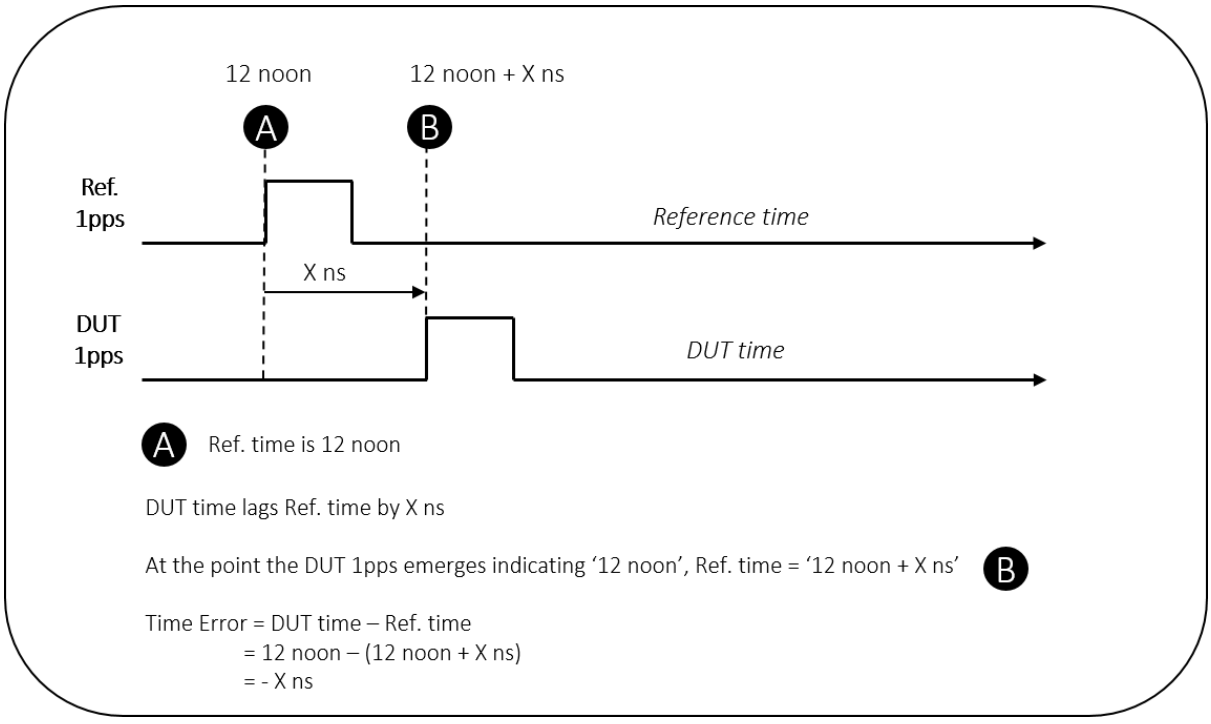


Figure 1

In summary, when interpreting a 1pps measurement result;

A **negative** value means the DUT **lags** the Reference.

A **positive** value means the DUT **leads** the Reference.

1588 Time Error measurement

The G.810 reference shown previously also applies when performing Time Error measurements on a 1588 flow. G.8273 Annex A discusses performing Time Error measurements on 1588 devices. This annex discusses the case for all types of 1588 devices, Grandmasters (GM), Boundary clocks (T-BC), etc. The text below will consider the case of a T-BC, however, the logic is also directly applicable when assessing performance of Grandmaster Clock devices.

The three primary measurements that can be performed on the egress 1588 from a T-BC are;

- ***T1 Time Error***: The difference (error) in the T1 timestamp compared to the Reference Time at the instant the Sync message egresses the T-BC.
- ***T4 Time Error***: The difference (error) in the T4 timestamp compared to the Reference Time at the instant the Del_Req ingresses the T-BC.
- ***Two Way (2W) Time Error***: The Time Error when the two-way protocol is utilised.

The *2W Time Error is the most important result* as this is the error seen by the downstream terminating devices when it processes the 1588 flow.[1]

G.8273 provides the following equations (Fig.2) for the calculation of Time Error on egress 1588 flows.

T1 Time Error : $TE_1 = T_1 - T_{1REF}$ (Eq. A.1.1)

T4 Time Error : $TE_4 = T_4 - T_{4REF}$ (Eq. A.1.3)

Two-Way (2W) Time Error : $\frac{|\langle TE_1(n)\rangle + \langle TE_4(m)\rangle|}{2} < X_{constant}$ (Eq. A.1.10)

where

T_1 = timestamp in the egress Sync message.

T_{1REF} = the time recorded from the Ref. when the Sync egresses the DUT.

T_4 = timestamp in the egress Delay Response message.

T_{4REF} = the time recorded from the Ref. when the Delay Request ingresses the DUT.

$X_{constant}$ = combined Time Error of the DUT.

Figure 2

[1] *It is also important to verify that the Time Error produced on the 1pps output from a T-BC accurately reflects the Time Error on the egress 1588. While the egress flow is the method of transferring time, once deployed in the network, the 1pps will be used to monitor the phase performance of the network equipment without having to disrupt the network connections.*

Telecom Boundary Clock (T-BC) model

Figure 3 shows the conceptual model of a T-BC and potential sources of Time Error.

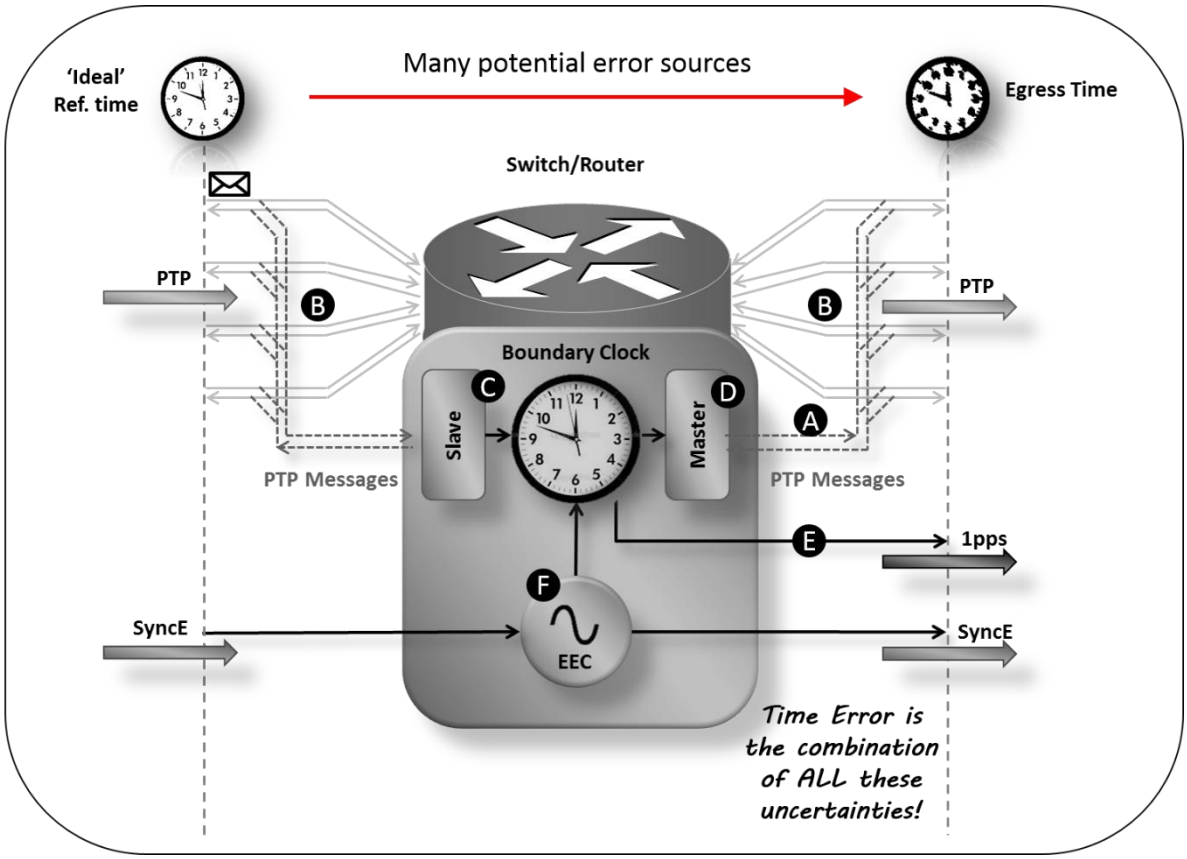


Figure 3

Time Error of a Boundary Clock (T-BC) is the **difference** of the time on the egress interface to that of the Ref. time supplied to the T-BC by the ingress 1588[2]. The Time Error observed will be the combined effect of **all** the relevant inaccuracies in the T-BC. Sources of inaccuracy include;

A	Traffic load and/or Packet Delay Variation (PDV) could delay 1588 packet.
B	Asymmetry; forward & reverse paths should be equal & opposite.
C	The error between the internal time recovered from the ingress 1588 and the Ref. time.
D	Time taken to/from egress versus internal struck time.
E	1pps should accurately reflect the egress PTP.
F	Frequency lock e.g. SyncE may be unstable.

[2] *Care should be taken when comparing the 1588 approach to time transfer to the measurement of, for example, T1 Time Error i.e. considering the point in time the T1 emerges from the DUT as time 'T2' as defined in the 1588 time transfer algorithm.* ***This is not the measurement being performed*** *i.e. it is not 'T2-T1' that is being assessed. What is being assessed is the accuracy of 'T1' when it emerges from the DUT with respect to the Ref. time.*

Polarity of 1588 Time Error components

The 1pps example shown earlier (Fig.1), indicates the polarity of Time Error on both the 1pps output and on the packet interface when the DUT's internal clock is *lagging* the Reference clock.

Figure 4 gives an example of the impact of *inaccurate* compensation of Sync transit time within a T-BC on Time Error on the egress 1588;

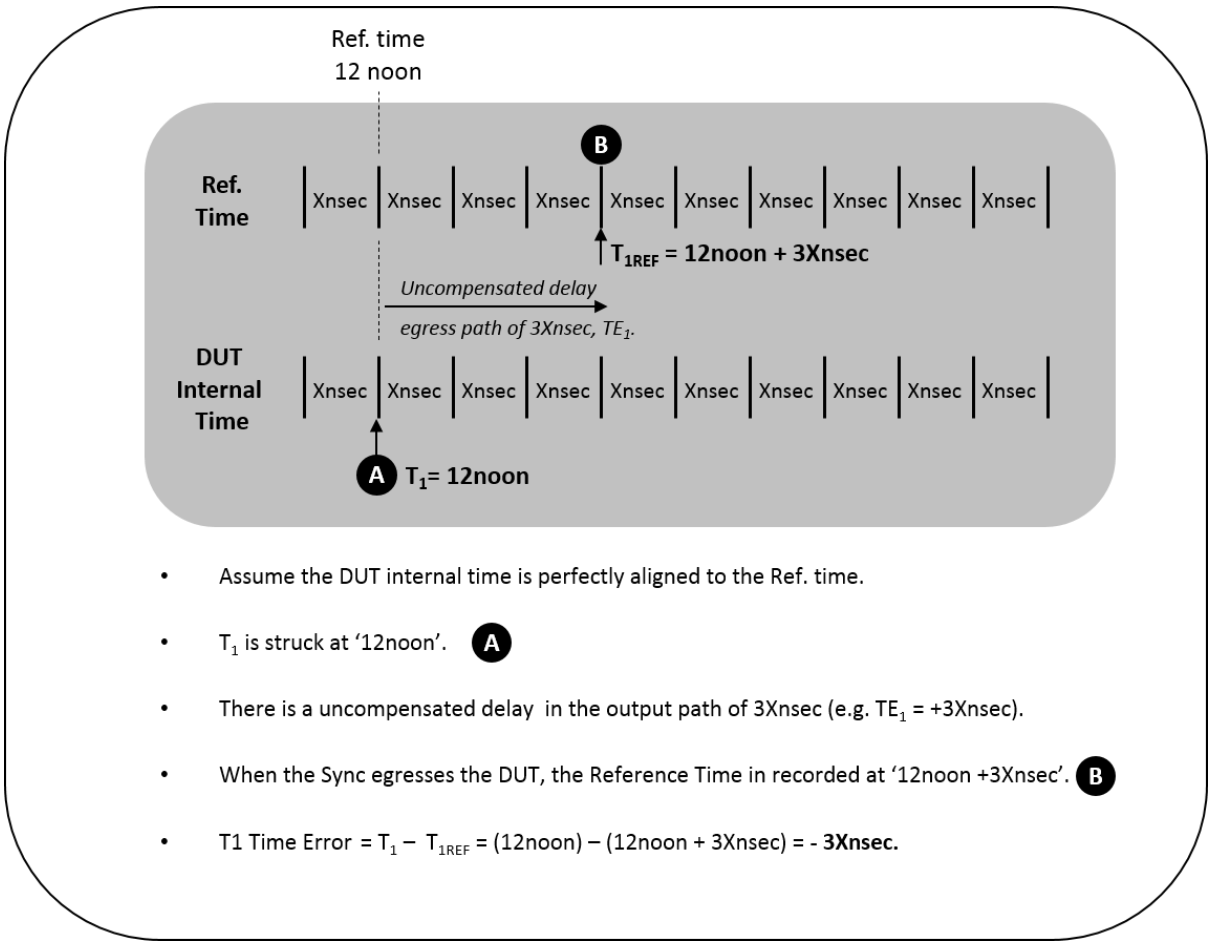


Figure 4

A similar exercise can be performed to assess the impact of inaccurate compensation of Delay Request transit time within a T-BC. The results are shown in the summary table below.

The measured performance[3] of a T-BC will be the **combination** effect of all error sources, including the Time Error in the Internal Time and the uncompensated delays in the output paths. In some cases, these factors combine to effectively compensate for one another.

[3] *When debugging equipment, comparing and contrasting the 3 Time Error results (2W, T1 & T4 Time Error) from the 1588 egress interface with that from the 1pps Interface, if present, can be useful to understand which potential source/s of error are the primary factors impacting the overall T-BC performance i.e. the 2W Time Error.*

Summary of T-BC Time Error inaccuracies

1pps Output interpretation

If the T-BC Internal time **lags** the Reference Time, a **negative** Time Error is produced.

If the T-BC Internal time **leads** the Reference Time, a **positive** Time Error is produced.

Egress 1588 Time Error interpretation

T-BC Internal time wrt Ref. time, impact on 2W, T1 & T4 Time Error.

T-BC **lags** the Ref. time, a more **negative** Time Error is produced.

T-BC **leads** the Ref. time, a more **positive** Time Error is produced.

T1 Time Error: Inaccurate delay compensated in the Sync transit time has the effect of;

Under compensation produces a more **negative** Time Error result.

Over compensation produces a more **positive** Time Error result.

T4 Time Error: Inaccurate delay compensated in the Del_req transit time has the effect of;

Under compensation produces a more **positive** Time Error result.

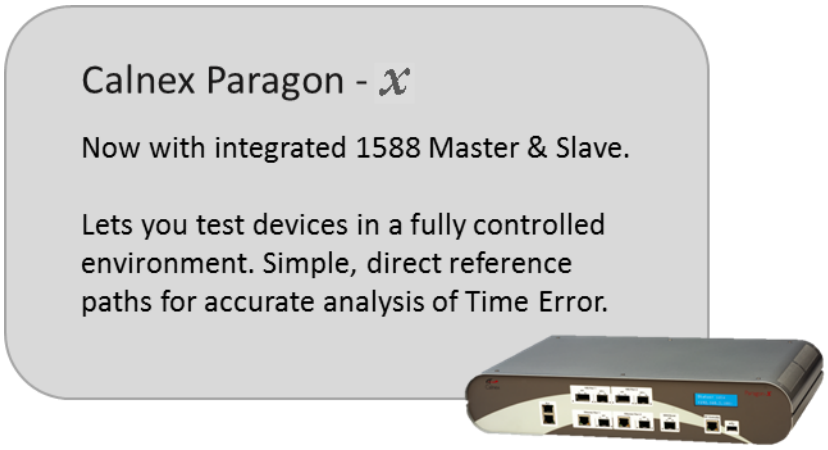
Over compensation produces a more **negative** Time Error result.

2W Time Error: Two-way calculated using (T1 Time Error + T4 Time Error)/2.

The polarity impact of T1 & T4 Time error on 2W Time Error can be deduced by applying the above statements to this equation.

Summary table

	Inaccuracy Source					
Time Error measurement	Internal time		Sync. transit time		Del_Req transit time	
	Lags Ref.	Leads Ref.	Under comp.	Over comp.	Under comp.	Over comp.
1pps	-ve	+ve	na	na	na	na
T1 Time Error	-ve	+ve	-ve	+ve	na	na
T4 Time Error	-ve	+ve	na	na	+ve	-ve
2W Time Error	-ve	+ve	-ve	+ve	+ve	-ve



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