Calnex
Insight and Innovation

ITU-T G.8273.2 Boundary Clock Testing

- Noise Generation
- Noise Tolerance
- Noise Transfer

Technical Brief

The accuracy of Telecom Boundary Clocks (T-BCs) is essential to the successful roll-out of LTE-A and TDD-LTE. The ITU-T has agreed a new specification for the performance of T-BCs, recommendation G.8273.2. This application note describes what a boundary clock is, and explains the critical performance parameters defined in G.8273.2.

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1 Introduction to Clocks

1.1 What is a clock?

In terms of network synchronisation systems, a clock is defined as 'a generator of the frequencies which will be used to synchronise the network". A master clock generates a frequency through some physical mechanism (e.g. the atomic transitions in a Caesium atom, or the resonance of a quartz crystal). A slave clock, on the other hand, receives a timing signal at its input and generates output signals locked in their frequency and phase relationship to the input.

1.2 Timing Signals

In most synchronisation systems, timing signals are periodic digital signals, where the edges of the signal are reference points in time known as the 'significant instants" of the signal. Ideally, these significant instants are precisely equally spaced in time, but in real systems there are small fluctuations in the positions of the significant instants. These fluctuations are called 'jitter" and 'wander", and are shown in Figure 1:

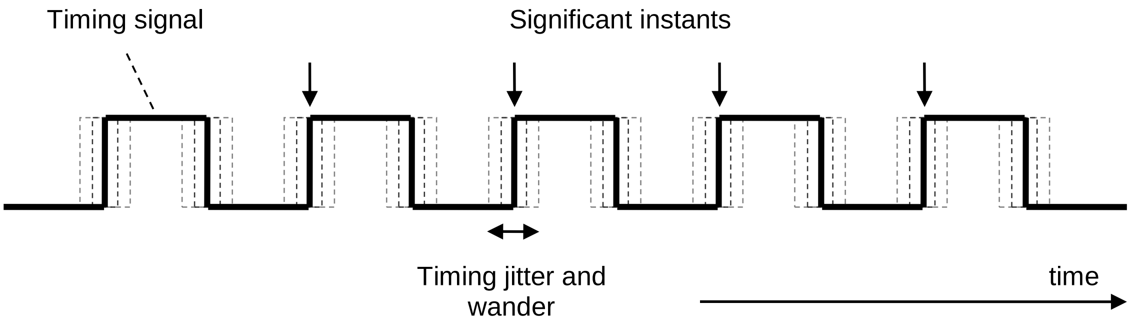


Figure 1: Conventional Timing Signal

The difference between jitter and wander is solely the frequency at which they occur: short-term, fast variations in position are called jitter, while longer term, slow movements are called wander. An arbitrary boundary is that jitter is above 10Hz, while wander is below 10Hz.

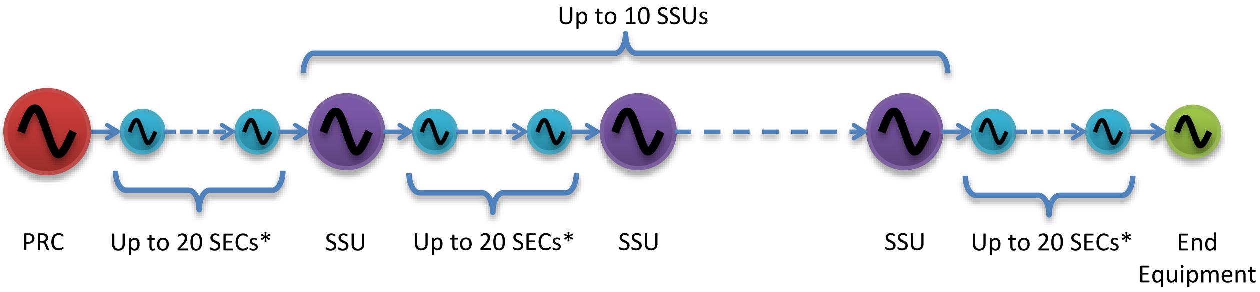
Clocks are designed to filter jitter and wander on their input. A clock acts as a low-pass filter, removing higher frequency variations from the input signal. The bandwidth of the clock indicates the extent to which a clock will remove noise from the input signal. Inevitably however, each clock will also add some 'noise" of its own.

1.3 Synchronisation Systems

A synchronisation system consists of a chain of clocks, distributing the reference frequency for the network generated by the master clock. Each clock in the chain is a slave clock, receiving an input frequency or 'timing signal" from the previous clock in the chain, and generating an output locked to that input frequency (i.e. at the same frequency or a fixed frequency relationship to the input).

As the timing signal progresses down the chain, the amount of noise (or phase error) increases. To control the noise generated by the chain, occasional 'clean-up" filters are required to remove the noise generated along the chain up to that point. An example of a chain of clocks is the SDH synchronisation reference chain, defined in G.803 and shown in Figure 2. It contains three types of clocks:

- **Primary Reference Clock (PRC)** – this is a master clock generating an accurate frequency to control the entire network. Typically it is a Caesium atomic clock, with a frequency accuracy of better than 1 part in 10^{11} when compared to UTC
- **Synchronisation Supply Unit (SSU)** – this is a slave clock with a low pass filter of 3mHz, removing any 'noise" accumulated along the chain. These are placed at regular intervals, to clean up the timing signal before passing it on
- **SDH Equipment Clock (SEC)** – this is the clock present in each network element. Its purpose is both to provide the frequency signals required for the network element to work correctly, and to pass on the frequency signals to the next element in the chain.



** No more than 60 SECs allowed in any one chain*

Figure 2: G.803 Synchronisation Reference Chain

1.4 Clock Specifications

ITU clock specifications define the clock performance in terms of five main parameters:

- **Noise generation** – the intrinsic noise generated by the clock itself.
  This is typically measured by applying an 'ideal", noise-free reference at the input, and comparing this reference to the output
- **Noise tolerance** – the maximum amount of noise the clock can tolerate at its input
- **Noise transfer** – this shows how much noise at the input is filtered out by the clock. It is usually defined as the clock bandwidth
- **Short term transient response** – the phase error generated during a switchover from one input reference to another (e.g. in the event of a reference failure)
- **Long term transient response or holdover** – the performance of the clock in the event of a total loss of input reference

2 Packet-based Clocks

2.1 Packet Timing Signals

A packet timing signal is similar in concept to a digital timing signal. The frequency is encoded as a series of time-critical packets in a network, known as 'event packets". It is the position of these packets in time that is important, not the contents of the packets. The packet timing signal still contains significant instants (normally the front edge of the packet), with a defined ideal position in time. The variation of the significant instants around their ideal position is termed 'packet delay variation" (PDV). This is shown in Figure 3:

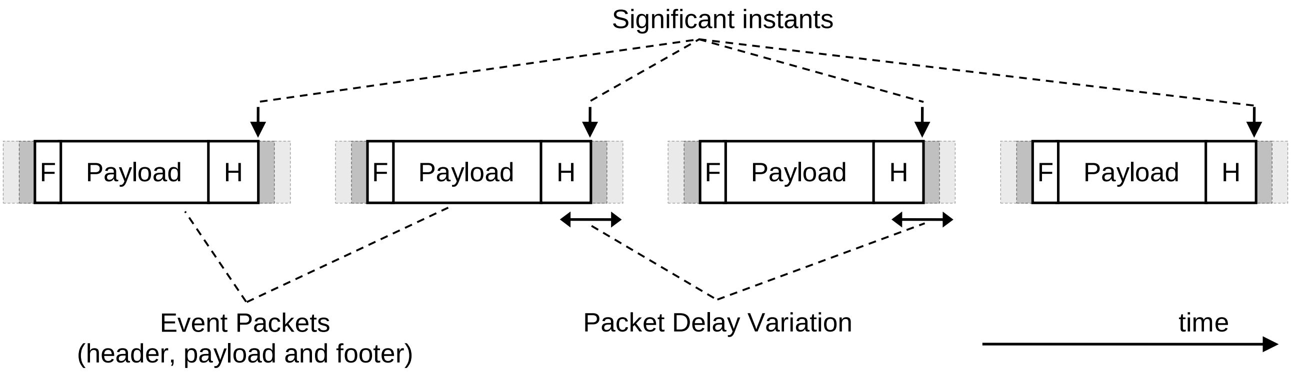


Figure 3: Packet Timing Signal

Some packet timing signals may be periodic (e.g. circuit emulation packets containing constant bit rate data), and for these the ideal position in time is implicitly given by the packet rate. Other packet timing signals are not periodic (e.g. PTP or NTP), and for these the ideal position in time is given by a timestamp embedded in the packet data.

2.2 Two-way Timing Protocols

While a uni-directional packet timing signal can be used to distribute frequency, a two-way timing signal is required to distribute time. Network time distribution protocols such as NTP (Network Time Protocol, defined in RFC5905) and PTP (Precision Time Protocol, defined in IEEE1588-2008) use a two-way exchange of timed messages to communicate time from a master node to a number of slave nodes.

For example, PTP uses the following message exchange, shown pictorially in Figure 4. NTP uses the same principle, although the message exchange protocol is different:

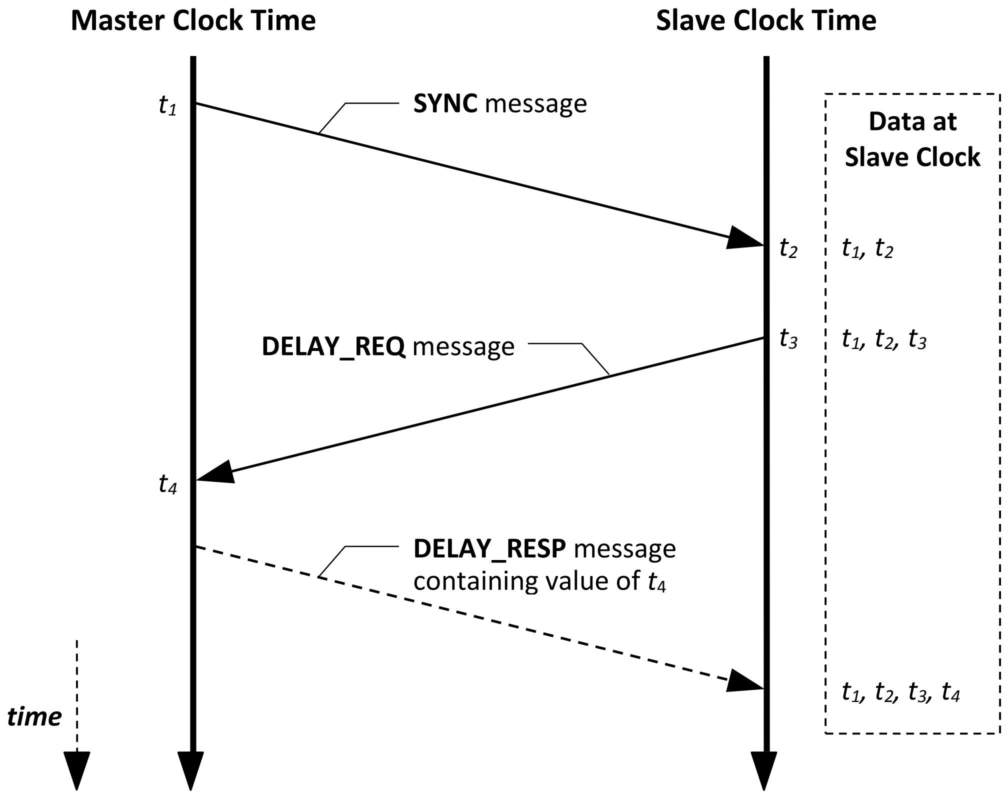


Figure 4: PTP Message Exchange

The messages yield four timestamps (t_1, t_2, t_3 and t_4) as shown in Figure 4. From these it is possible to calculate the round trip time for messages from the master to the slave, and back to the master (assuming that the slave clock is advancing at a similar rate to the master). The time offset at the slave may then estimated using the assumption that the one-way network delay is half the round trip delay.

Note that if the forward and reverse paths are of different lengths, then this will introduce an error into the time offset estimate. There is no information within the PTP protocol itself which allows the offset to be corrected for this asymmetry, although the slave may be able to make use of other information available to infer the size of the offset.

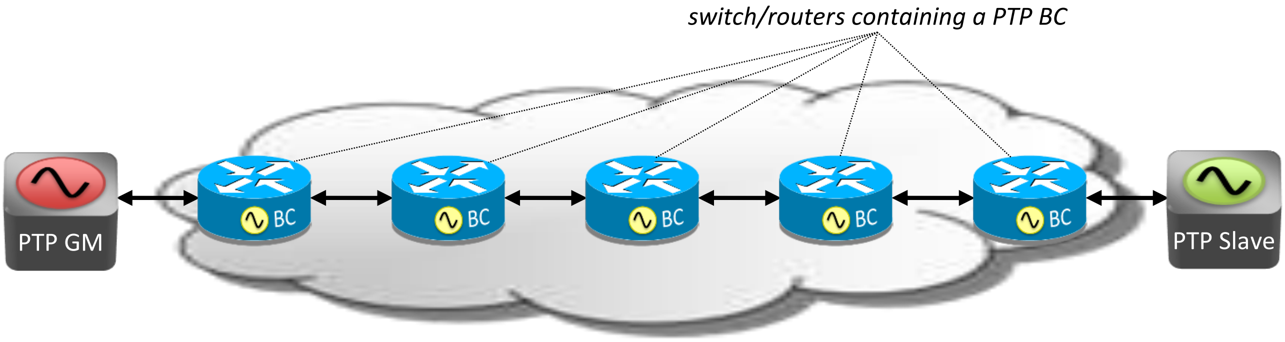
2.3 Packet Timing Clocks

PTP defines four main clock types:

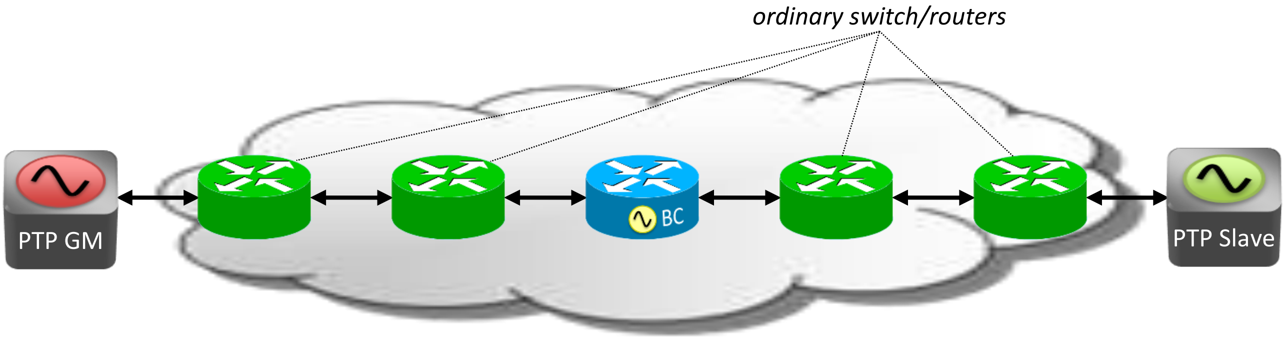
1. **Grandmaster clock** – the principal source of time and frequency to the synchronisation system.
2. **Slave clock** – a clock terminating the PTP protocol, and supplying time or frequency to the end application.
3. **Boundary clock** – a network node clock, receiving time from the grandmaster, and passing this on down the chain to subsequent network elements. In effect, a boundary clock consists of a PTP slave port and one or more PTP master ports.
4. **Transparent clock** – a network node clock, calculating a ‘residence time” for each PTP event message. This residence time is a record of how long it took for the message to be forwarded to the next node, and is used to calculate the delay of the message as it passes through the network.

2.4 Packet Timing Systems

The ITU-T is in the process of defining two ‘profiles” for the distribution of time across the network using PTP. The first is for the case where every node in the path between the master and the slave contains a BC. This is termed ‘full timing support”. The second is where there may be a mixture of ordinary switches and routers, and ‘PTP aware” devices, containing a BC or TC. This is known as ‘partial timing support”.



Full Timing Support (G.8275.1):
every switch/router on the path between GM and slave contains a PTP Boundary Clock



Partial Timing Support (G.8275.2):
not all switch/routers on the path between GM and slave contain a PTP Boundary Clock

Figure 5: Full and Partial Timing Support

3 Boundary Clocks for Full Timing Support

The ITU-T has defined a clock specification for the telecom boundary clock (T-BC) to be used in the G.8275.1 profile for full timing support. This clock specification is defined in the draft recommendation G.8273.2. It follows the same approach as the earlier clock specifications, with the five key elements of noise generation, noise transfer, noise tolerance, transient response and holdover.

In terms of a PTP time clock, the term 'noise" means 'time error". It is characterised using the three parameters:

- Maximum absolute time error (max |TE|) – the maximum difference from the reference clock, either positive or negative. This is measured on the unfiltered data.
- Constant time error (cTE) – a fixed offset from the reference clock, e.g. such as might be produced by delay asymmetry within the device.
- Dynamic time error (dTE) – the variation of time error with respect to the reference, measured using the metrics MTIE and TDEV. The data is filtered using a 0.1Hz low-pass filter.

These terms are defined in ITU-T Recommendation G.8260 (Amendment 2), and described in more detail in the Calnex white paper "Time and Time Error: An Overview".

3.1 Functional Model

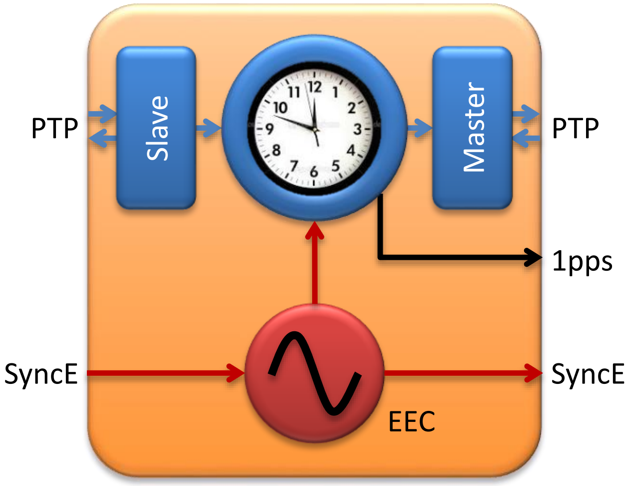


Figure 6: Telecom Boundary Clock (T-BC)

As mentioned earlier, a PTP boundary clock has at least two ports. The first is a PTP slave port, receiving timing from an upstream master. The clock is synchronised to this source of time. The other port(s) are PTP master ports, supplying time to downstream clocks. In the G.8273.2 specification, a T-BC may also make use of a stable frequency source such as Synchronous Ethernet to help stabilise the clock.

3.2 Time Error Generation

This is a measure of the intrinsic amount of 'noise" (or time error) introduced by the T-BC. It is defined as the time error at the output of the device with an ideal signal on the input, as shown in Figure 7. The specification applies to both the 1pps and the PTP outputs of the T-BC.

G.8273.2 specifies two classes of performance for time error generation: class A, for use in shorter chains of T-BCs, and class B, which is expected to be used in longer chains of around 20 nodes.

G.8273.2 defines limits on time error generation in terms of all three parameters, maximum absolute time error (max |TE|), constant time error (cTE) and dynamic time error (dTE).

For maximum time error, the limit is 100ns for a class A device, and 70ns for a class B device. These limits apply to the 'raw" unfiltered time error measurement.

For constant time error class A clocks must have cTE less than 50ns, while class B clocks must have cTE less than 20ns.

For dynamic time error, both class A and class B clocks must have dTE of less than 40ns peak to peak, measured over at least 1000s. This is governed by an MTIE mask. G.8273.2 also defines a TDEV limit of 4ns at observation intervals up to 1000s. A 0.1Hz low-pass filter is applied to the raw time error measurements before calculating MTIE and TDEV.

TDEV measures the variability of a signal over different observation intervals, whilst MTIE measures the peak-to-peak swings over different observation intervals. Therefore MTIE is a good indicator of the maximum change in error, while TDEV is more useful for understanding the noise accumulation of a chain of clocks.

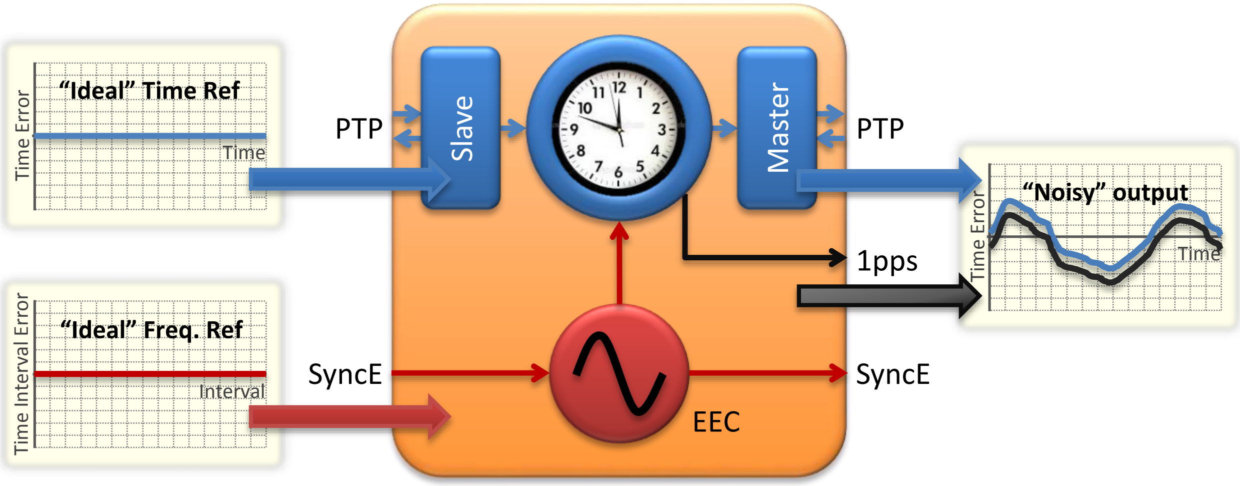


Figure 7: T-BC Time Error Generation

3.3 Time Error Tolerance

Time error tolerance is the maximum amount of time error a clock is required to tolerate on its inputs. A T-BC has both SyncE and PTP inputs, and may expect both of these to be ‘noisy” in a real deployment. Therefore time error tolerance is defined with ‘noise” on both inputs simultaneously, as shown in Figure 8.

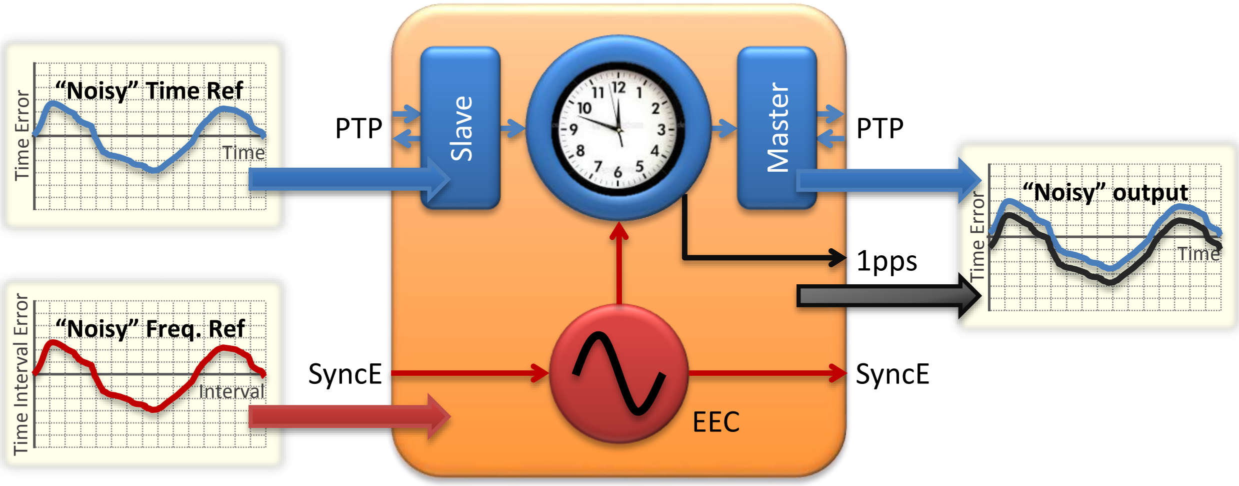


Figure 8: T-BC Time Error Tolerance

The output time error is not specified for a time error tolerance test. This is standard practice for a clock that is part of a chain. The output time error is characterised by the time error generation test, and it is not necessary to prove this again. Therefore the objective of the time error tolerance test is to prove that the clock works normally without attempting to switch references or generate alarm messages.

The maximum amount of noise that should be tolerated on the PTP input is defined by the dTE mask for the network limit, defined in G.8271.1. This is shown in Figure 9:

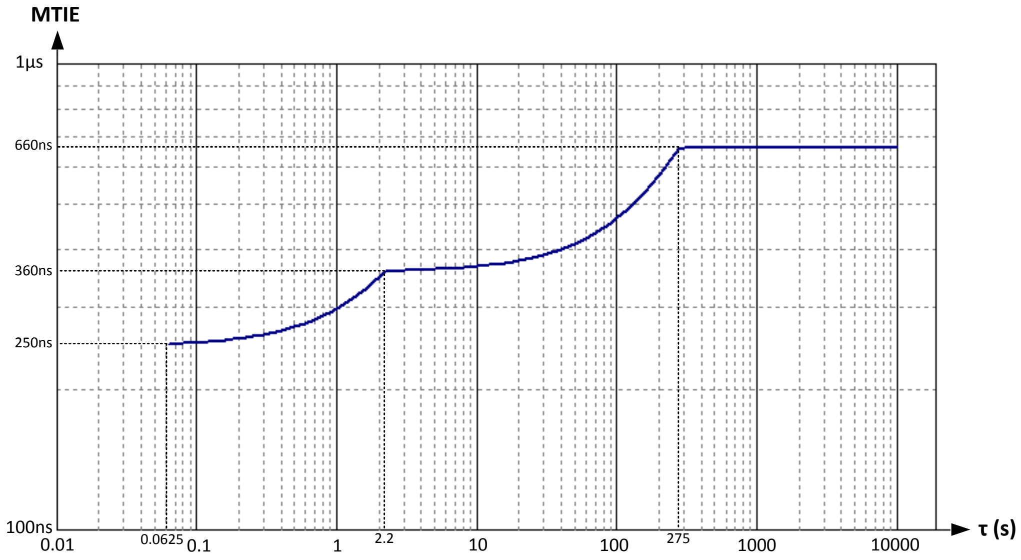


Figure 9: MTIE mask for dTE network limit

The maximum amount of noise that should be tolerated on the SyncE input is defined in G.8262 (clause 9). The method to test it is also discussed in G.8262.

3.4 Time Error Transfer

Time error transfer is a measure of how much noise present at the input is transferred to the output of the clock. It is usually expressed in terms of a filter bandwidth.

There are two filter characteristics to measure. The first is the time error transfer from PTP to PTP (and also PTP to 1pps), i.e. the boundary clock itself. This is defined in G.8273.2 to be a low-pass filter with a bandwidth of between 0.05 and 0.1Hz, as shown in Figure 10:

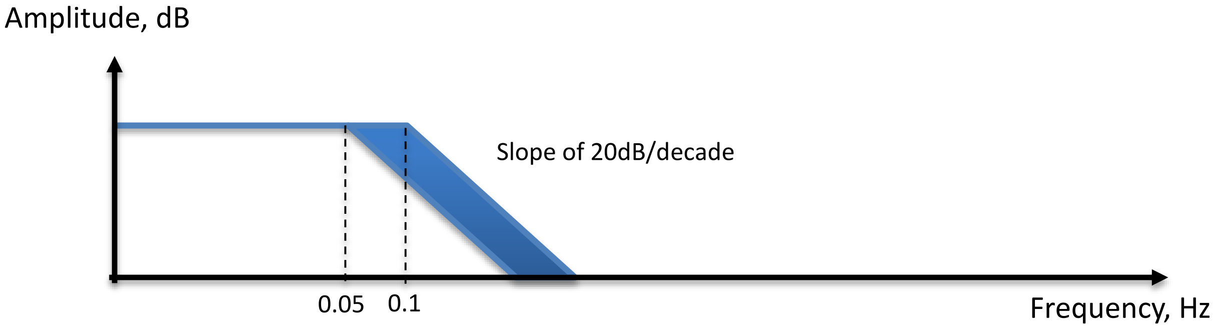


Figure 10: PTP to PTP Transfer Function

The transfer function from the SyncE input to PTP output is more complex. Firstly, there is a low-pass function in the EEC itself, defined in G.8262 to have a bandwidth of between 1 and 10Hz. The boundary clock then acts as a high-pass filter to the SyncE signal, at the same bandwidth as the PTP to PTP low pass filter. This high-pass function as a natural consequence of the way the clock works: it smooths out high frequency noise by following the local frequency reference (in this case, the SyncE), while following the PTP input at low frequencies.

The net result is that any noise (or phase wander) on the SyncE input is band-pass filtered, as shown in Figure 11:

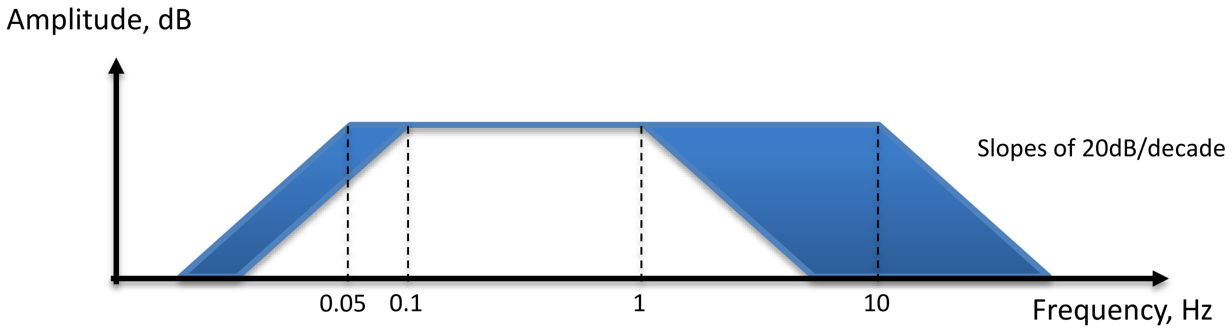


Figure 11: SyncE to PTP Transfer Function

The filter characteristics can be verified by applying sinusoidal tones at different frequencies to the inputs, and observing the attenuation of those tones at the output, as shown in Figure 12. For example, if a 1Hz sinusoidal time error was applied at the PTP input, the output should be attenuated by approximately 10 times. However, a 0.01Hz tone should not be attenuated by the clock.

For the SyncE to PTP transfer function three tones should be used, one below the pass-band, one in the middle, and one above the pass-band.

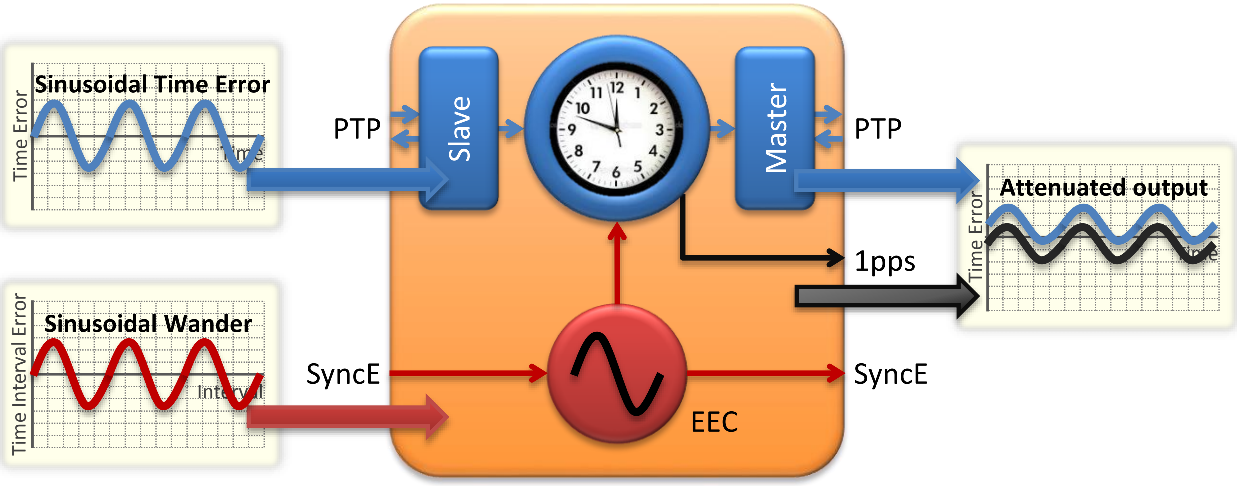


Figure 12: T-BC Time Error Transfer

3.5 Short-term Transient Response

Short-term transient response refers to the time error generated when a clock switches over from one input reference to another, e.g. in the event of a reference failure. Currently G.8273.2 does not define the short-term transient response for a T-BC.

However, there is a second related specification defined in Annex B of G.8273.2. If a transient is received on the SyncE input of the T-BC (e.g. to a re-arrangement in the previous network element), this transient phase wander may produce significant time error in the T-BC output. Therefore a T-BC must reject this transient on its input.

It can achieve this by monitoring the ESMC messages on the SyncE interface. These report the QL (Quality Level) of the SyncE signal, and indicate when the signal is temporarily not traceable to a primary reference clock. On receipt of a degraded QL, the T-BC must stop using the SyncE signal, and rely instead on its own local oscillator. When traceability of the SyncE signal is restored, the T-BC can go back to using the SyncE signal.

Annex B defines the following mask for the clock output in the event of a transient on the SyncE input:

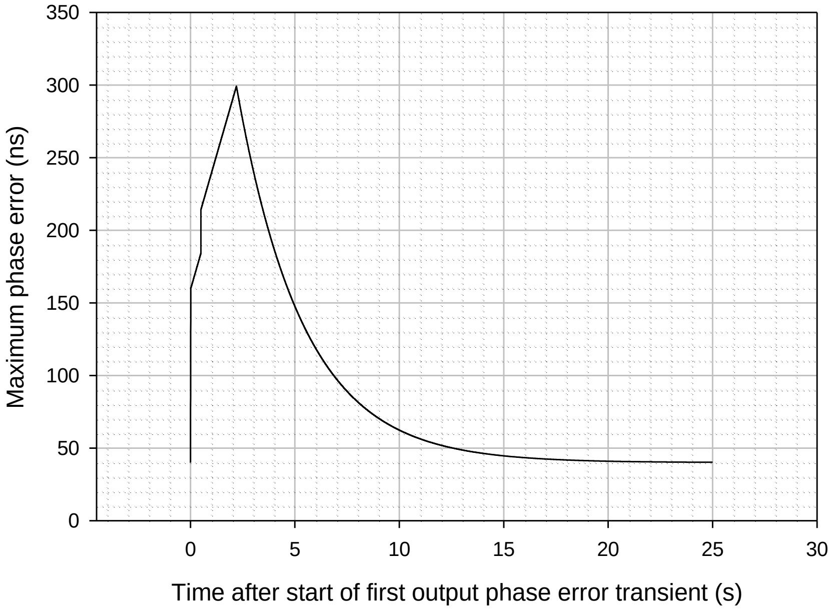


Figure 13: Phase error mask during a SyncE transient (Figure B.1 from Annex B)

The method to verify compliance with the mask shown in Figure 13 is still under discussion in ITU-T.

3.6 Long-term Transient Response (Holdover)

The long term-transient response (sometimes known as holdover) defines the performance of the clock in the event of a loss of the input references, when there is no viable alternate reference to switch to. For a T-BC, this may be assisted holdover, using the SyncE signal to maintain the timebase of the clock advancing at a stable rate.

G.8273.2 does not currently define a performance requirement for a T-BC in holdover or assisted holdover.

4 Further Reading

The following documents contain the various clock specifications defined by the ITU-T:

1. ITU-T Recommendation G.811: ‘Timing characteristics of primary reference clocks”, September 1997
2. ITU-T Recommendation G.812: ‘Timing requirements of slave clocks suitable for use as node clocks in synchronization networks”, June 2004 *(SSU clock specification)*
3. ITU-T Recommendation G.813: ‘Timing characteristics of SDH equipment slave clocks (SEC)”, March 2003
4. ITU-T Recommendation G.8260: ‘Definitions and terminology for synchronisation in packet networks: Amendment 2”, expected publication May 2014.
5. ITU-T Recommendation G.8262: ‘Timing characteristics of a synchronous ethernet equipment slave clock”, July 2010
6. ITU-T Recommendation G.8263: ‘Timing characteristics of packet-based equipment clocks”, February 2012 *(PTP clock for frequency synchronisation of mobile basestations to within 50ppb)*
7. ITU-T Recommendation G.8273.2: ‘Timing characteristics of telecom boundary clocks”, expected publication May 2014 *(PTP boundary clock for time synchronisation of mobile basestations to within 1.5μs)*

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