The importance of measuring wander on high speed interfaces

We're often asked that if the 1G and 10G interfaces on a device meet ITU-T G.8262 performance targets, and with good margin, why is it also necessary to test the performance of the 40G and 100G interfaces?

It's a good question and one that deserves a clear explanation. As a rule, devices such as Ethernet switches or routers employ a single, high-stability oscillator that is used as the reference source of frequency to all physical outputs from the device. The performance of this reference oscillator will be a primary source of wander on all outputs (at all rates), but importantly, it's not the *only* source in a switch/router. If it was, it would be reasonable to assume that the wander measured on all the interfaces would be very similar and directly correlate to the oscillator's performance.

So what else contributes to wander in Ethernet equipment? It is typical for the reference oscillator to run at a relatively low rate, for example, 10 MHz. Running at a low rate reduces clock noise and provides straightforward locking to external references like a 10 MHz signal from a GNSS input.

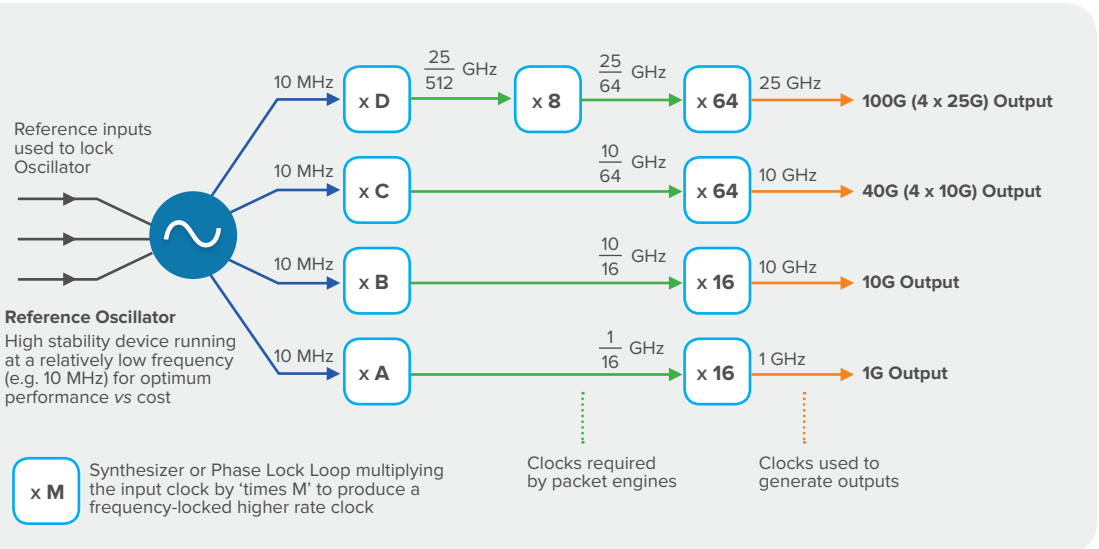
However, irrespective of the frequency of the reference oscillator, multiple synthesizers and Phase Lock Loops (PLLs) are still required. These are used to multiply the reference frequency to supply all the various interface rates supported by the equipment, as well as supplying the various clock rates required by the equipment's internal data processing engines. Crucially, each synthesizer and PLL has the potential to add wander noise to the outputs they supply and hence this is the primary source of *variable* wander performance between different interface types.

As the primary frequency of the interface increases, the more complex the synthesizers and PLLs and the greater the potential for wander and locking issues. When dealing with very high speed interfaces like those at 40G and 100G, the challenge of managing and processing such high speed data means that very wide bus architectures may be employed within the ASIC or custom silicon components, for example, 128/256/512 bit wide buses or even greater.

As data is passed between these high-density silicon components, the bus width may have to be reduced to enable the tracking of such large bus structures around the PCB. This leads to the clock rates *between* the components being different to the clock rates used *inside* the components. To support this, the path of the clock from say a 10 MHz reference oscillator to a 25G line clock may be through multiple synthesizers/PLLs. And any wander and/or locking issues within any of these synthesizers/PLLs will lead to different wander generation performance on the high speed interface compared to that present on other lower speed interfaces.

The bottom line is that higher interface rates inherently increase the design challenges. It therefore follows that full testing of each type of high speed interface is required to ensure the performance of each synthesizer/PLL is known and proven when qualifying an Ethernet switch or router in order to achieve G.8262 Standards conformance.

Conceptual example of the clock generation inside a switch or router



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